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72242 (6653)

Amendments to the Claims:

A1 sub B1

1. (currently amended): A method of integrated circuit design [said method] comprising [the] steps of:
 - (a) placing and wiring an integrated circuit design;
 - (b) generating a slack graph to identify [a] identifying critical paths in an integrated circuit design;
 - (c) removing non-critical paths from the slack graph;
 - (d) calculating a corresponding traversal weight for each edge [b] weighting edges] in the [identified said] critical paths;
 - (e) assigning a net weight value [c] assigning net criticality] to each [weighted] edge in the critical paths from the corresponding traversal weight [responsive to edge weight]; and
 - (f) [d] re-placing and wiring nets according to the net weight value to eliminate the critical paths from the integrated circuit design [edge criticality].

2-3. (canceled)

4. (currently amended): A method of integrated circuit design comprising steps of:
 - (a) placing and wiring an integrated circuit design;
 - (b) identifying critical paths in the integrated circuit design;
 - (c) calculating a corresponding traversal weight for each edge in the critical paths;
 - (d) assigning a net weight value to each edge in the critical paths from the corresponding traversal weight; and
 - (e) re-placing and wiring nets according to the net weight value to eliminate the critical paths in the integrated

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circuit design [~~a method as in claim 3~~] wherein step (b) of identifying critical paths comprises forming a slack graph indicating path slack and edges within the [said] critical paths and removing [~~7~~] non-critical paths [~~being deleted~~] from the [said] slack graph.

5. (currently amended): A method as in claim 4 wherein step (c) [~~of weighting edges~~] comprises [the] steps of:

(c1) [~~i~~] traversing each [said] critical path [paths] from front to back and assigning [~~7~~] an input path weight for [~~being assigned to~~] each edge encountered in traversing each critical path [said traversal];

(c2) [~~ii~~] traversing each critical path from back to front and assigning [~~7~~] an output path weight for [~~being assigned to~~] each edge encountered [edge] in traversing each critical path [said reverse traversal]; and

(c3) [~~iii~~] summing the [said assigned] input path weight and the [said assigned] output path weight for each edge.

6. (currently amended): A method as in claim 5 wherein assigning a net weight [criticality] value comprises: sorting nets according to traversal [edge] weight into groups;

~~[grouping sorted nets;]~~ and
assigning a net weight [criticality] value to each of the groups [group].

7. (currently amended): A method as in claim 6 wherein the step (e) [~~(c)~~] of re-placing and wiring nets comprises:

(e1) [~~+~~] selecting an edge having a highest traversal

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weight [criticality] value;

(e2) [iii]) adjusting cell placement and net wiring for
the [said] selected edge; and

(e3) [iii]) checking for remaining critical edges and
repeating steps (e1) and (e2) [i-ii] until no critical edges
are found.

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8. (currently amended): A method as in claim 7
further including prior to [the step (iii) of] checking for
remaining critical edges a [the] step of [i-iiiA]) checking to
determine if exit criteria are met and ending if the [said]
exit criteria are met.

9. (currently amended): A computer-readable medium
having stored thereon a plurality of instructions, the
plurality of instructions including instructions which, when
executed by a processor, cause the processor to:

- (a) place and wire an integrated circuit design;
- (b) generate a slack graph to [a]) identify critical
paths in an integrated circuit design;
- (c) calculate traversal weights for [b) weight] edges in
the [identified said] critical paths;
- (d) [e]) assign a net weight value from the traversal
weights [net criticality to each weighted edge responsive to
edge weight]; and
- d) re-place and wire nets according to the net weight
value [edge criticality].

10-11. (canceled)

12. (currently amended): A computer-readable medium
having stored thereon a plurality of instructions, the

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plurality of instructions including instructions which, when executed by a processor, cause the processor to:

(a) place and wire an integrated circuit design;
(b) identify critical paths in the integrated circuit design;
(c) calculate a corresponding traversal weight for each edge in the critical paths;
(d) assign a net weight value from the corresponding traversal weights to each edge in the critical paths; and
(e) re-place and wire nets according to the net weight value to eliminate the critical paths from the integrated circuit design [A computer readable medium as in claim ~~ii~~]
wherein identifying critical paths comprises forming a slack graph indicating path slack and edges within the [said] critical paths and removing [-] non-critical paths [being deleted] from the [said] slack graph.

13. (currently amended): A computer-readable [computer readable] medium as in claim 12 wherein [step] (c) of weighting edges causes the processor to:

(c1) [ii] traverse each [said] critical path [paths] from front to back and assign [-] an input path weight for [being assigned to] each edge encountered in traversing each critical path [said traversal];

(c2) [iii] traverse each critical path from back to front and assign [-] an output path weight for [being assigned to] each edge encountered [edge] in traversing each critical path [said reverse traversal]; and

(c3) [iv] sum the [said assigned] input path weight and the [said assigned] output path weight for each edge.

14. (currently amended): A computer-readable

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[computer readable] medium as in claim 13 wherein assigning a net weight value [criticality] causes the processor to: sort nets according to traversal [edge] weight into groups; [group sorted nets,] and assign a net weight [criticality] value to each of the groups [group].

15. (currently amended): A computer-readable [computer readable] medium as in claim 14 wherein re-placing and wiring nets causes the processor to:

(e1) [i+] select an edge having a highest traversal weight [criticality] value;
(e2) [ii+] adjust cell placement and net wiring for the [said] selected edge; and
(e3) [iii+] check for remaining critical edges and repeating steps (e1) and (e2) [i-ii] until no critical edges are found.

16. (currently amended): A computer-readable [computer readable] medium as in claim 15 wherein if exit criteria are met, the [said] processor is caused to end prior to selecting and adjusting all critical edges.

17. (new): A method as in claim 1 wherein step (d) comprises identifying bottlenecks.

18. (new): A computer-readable medium as in claim 9 wherein (d) comprises identifying bottlenecks.